JML9061,JML9062,JML9064
JML9061S,JML9062S,JML9064S

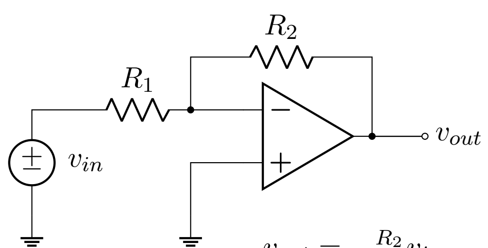
JML906x 10-MHz, RRIO, CMOS Operational Amplifiers

Features

- Rail-to-rail input and output
- Low input offset voltage: ±0.4 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: 14 nV/$\sqrt{\text{Hz}}$
- Low input bias current: ±1 pA
- Low quiescent current: 740 µA(MAX)
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8 V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version:JML906xS
- Internal RFI and EMI filter
- Extended temperature range: –40°C to 125°C
- compatibility AECQ-100

Applications

- E-bikes
- Smoke detectors
- HVAC: heating, ventilating, and air conditioning
- Refrigerators
- Motor control: AC induction
- Refrigerators
- Wearable devices
- Laptop computers
- Washing machines
- Sensor signal conditioning
- Power modules
- Barcode scanners
- Active filters
- Low-side current sensing



$$v_{out} = -\frac{R_2}{R_1} v_{in}$$

General Description

JML9061 (single),JML9062 (dual), andJML9064 (quad) are single-, dual-, and quad- low-voltage (1.8V to 5.5 V) operational amplifiers (op amps) with rail to rail input and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of theJML906x is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler.

XMO906xS devices include a shutdown mode that allow the amplifiers to switch into standby mode with typical current consumption less than 1 µA.

JML906xS family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

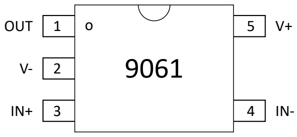
Device Information[1,2]

PART NUMBER	PACKAGE	BODY SIZE(NOM)
JML9061	SOT-23 (5)	1.60 mm × 2.90 mm
	SC70 (5)	1.25 mm × 2.00 mm
JML9061S	SOT-23 (6)	1.60 mm × 2.90 mm
JML9062	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	2.00 mm × 2.00 mm
JML9062S	VSSOP (10)	3.00 mm × 3.00 mm
JML9064	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm
JML9064S	WQFN (16)	3.00 mm × 3.00 mm

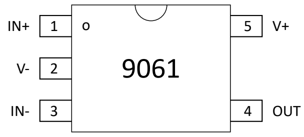
[1] For all available packages,see the orderable addendum at the end of the data sheet.
[2] Package is for preview only.

Pin Configuration and Functions

5-Pin SOT-23
(Top View)



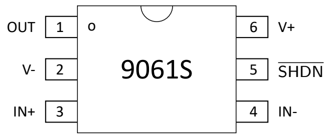
5-Pin SC70
(Top View)



Pin Functions:9061

PIN			I/O	DESCRIPTION
NAME	**SOT-23**	**SC70**		
IN+	3	1	I	Noninverting input
IN-	4	3	I	Inverting input
OUT	1	4	O	Out
V+	5	5	—	Positive (highest) power supply
V-	2	2	—	Negative (low) supply or ground (for single-supply operation)

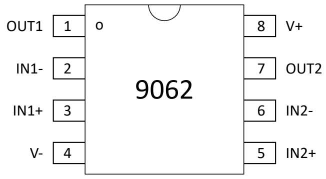
6-Pin SOT-23
(Top View)



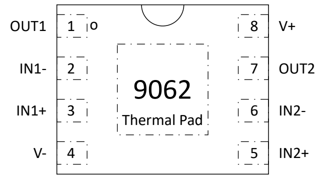
Pin Functions:9061S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN-	4	I	Inverting input
OUT	1	O	Out
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See Shutdown Function section for more information
V+	5	—	Positive (highest) power supply
V-	2	—	Negative (low) supply or ground (for single-supply operation)

8-Pin SOIC, VSSOP, TSSOP
(Top View)



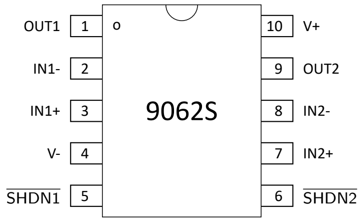
8-Pin WSON With Exposed Thermal Pad
(Top View)



Pin Functions: Pin Functions:9062

PIN		I/O	DESCRIPTION
NAME	**NO.**		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (low) supply or ground (for single-supply operation)

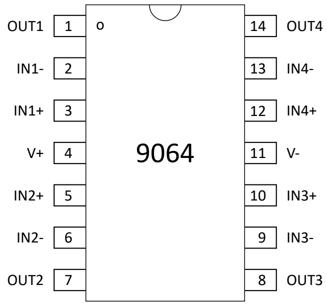
10-Pin VSSOP
(Top View)



Pin Functions: Pin Functions:9062S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	8	I	Inverting input, channel 2
IN2+	7	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	9	O	Output, channel 2
$\overline{\text{SHDN1}}$	5	I	Shutdown: low = amp disabled, high = amp enabled.Channel 1. See Shutdown Function section for more information
$\overline{\text{SHDN2}}$	6	I	Shutdown: low = amp disabled, high = amp enabled.Channel 2. See Shutdown Function section for more information
V+	10	—	Positive (highest) power supply
V-	4	—	Negative (low) supply or ground (for single-supply operation)

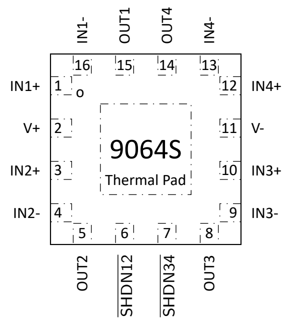
14-Pin SOIC, TSSOP
(Top View)



Pin Functions: Pin Functions:9064

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (low) supply or ground (for single-supply operation)

16-Pin WQFN With Exposed Thermal Pad
(Top View)



Pin Functions: Pin Functions:9064S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	16	I	Inverting input, channel 1
IN1+	1	I	Noninverting input, channel 1
IN2–	4	I	Inverting input, channel 2
IN2+	3	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
$\overline{\text{SHDN12}}$	5	I	Shutdown: low = amp disabled, high = amp enabled.Channel 1,2. See Shutdown Function section for more information
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled.Channel 3,4. See Shutdown Function section for more information
V+	2	—	Positive (highest) power supply
V-	11	—	Negative (low) supply or ground (for single-supply operation)

Specifications

Absolute Maximum Ratings

Over operating ambient temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage [(V+) – (V–)]			0	6	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current[2]		–1	10	mA
Output short-circuit[3]			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		-65	150	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
[3] Short-circuit to ground, one amplifier per package.

ESD Ratings

		VALUE	UNIT
9061 PACKAGES			
V_{ESD} Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[1]	±1500	
ALL OTHER PACKAGES			
V_{ESD} Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[1]	±1500	

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating ambient temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S= [V+] – [V–])	1.8	5.5	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
V_O	Output voltage range	V–	V+	V
V_{SHDN_IH}	High level input voltage at shutdown pin (amplifier enabled)	1.2	V+	V
V_{SHDN_IL}	Low level input voltage at shutdown pin (amplifier disabled)	V–	0.2	V
T_A	Specified temperature	–40	125	°C

Electrical Characteristics

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	input offset voltage	V_{os}=5V		±0.4	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±1.8	
dV_{os}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±0.5		μV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±7	±100	μV/V
	Channel separation, DC	At DC		134	140	dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	VS = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C	86	104		dB
		V_S = 5.5 V, – 0.1 V < V_{CM} < 5.6 V, T_A = –40°C to 125°C	60	87		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.5 V, T_A = –40°C to 125°C	88	108		
		V_S = 1.8 V, – 0.1 V < V_{CM} < 1.9 V, T_A = –40°C to 125°C		88		
INPUT BIAS CURRENT						
I_B	Input bias current			±1		pA
I_{OS}	Input offset current			±0.3		pA
NOISE						
E_n	Input voltage noise (peak to peak)			5.7		μVpp
e_n	Input voltage noise density	VS = 5 V, f = 10 kHz		15		$nV/\sqrt{Hz}$
		VS = 5 V, f = 1 kHz		20		
i_n	Input current noise density	f= 1 kHz		4		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			1.2		pF
C_{IC}	Common-mode			2.4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, , (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10kΩ	103	128		dB
		V_S = 5.5 V, , (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10kΩ	111	135		
		V_S = 1.8 V, , (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2kΩ		127		
		V_S = 5.5 V, , (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2kΩ		130		

Electrical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = +1		64		°
SR	Slew rate	V_S = 5 V, G = +1		7		V/μs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		0.5		μs
		To 0.01%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		0.9		
t_{or}	Overload recovery time	V_S = 5.5 V, V_{IN}* gain >V_S		0.6		μs
THD+N	Total harmonic distortion + noise[1]	V_S = 5.5 V, V_{CM} = 2.5 V, V_O= 1 V_{RMS}, G = +1,f = 1 kHz		0.00047%		
OUTPUT						
V_O	Output swing from supply rails	V_S = 5.5 V,R_L = 10 kΩ			6	mV
		V_O = 5.5 V,R_L = 2 kΩ			20	
I_{SC}	Short-circuit current	V_S = 5 V		±55		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V,I_O = 0mA		554	710	uA
		V_S = 5.5 V,I_O = 0mA,T_A = –40°C to 125°C			740	

[1] Third-order filter; bandwidth = 80 kHz at –3 dB.

Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

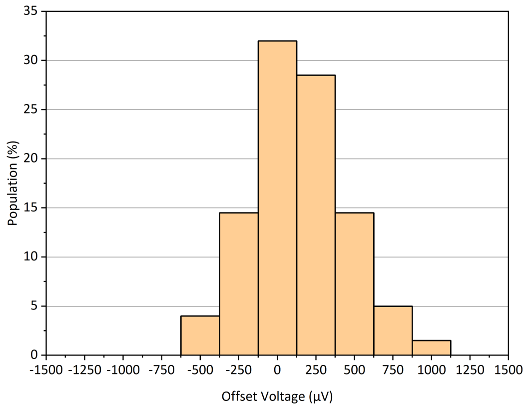


Figure 1: Offset Voltage Production Distribution

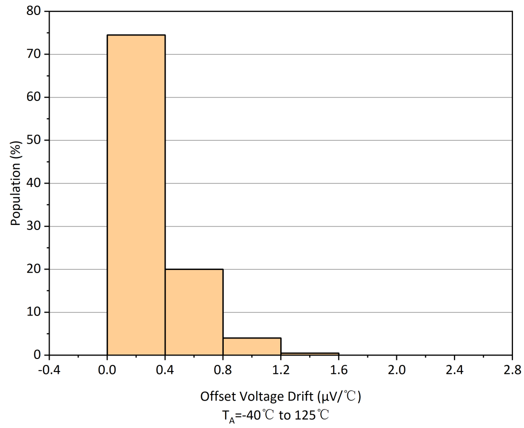


Figure 2: Offset Voltage Drift Distribution

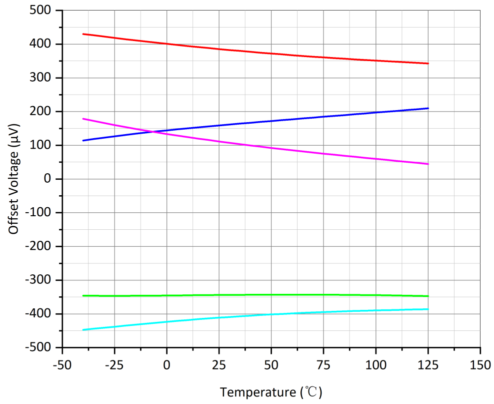


Figure 3: Offset Voltage vs Temperature

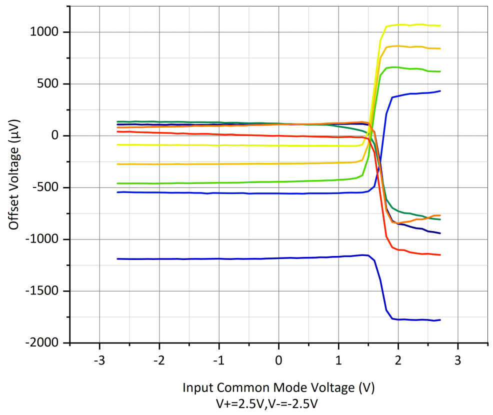


Figure 4: Offset Voltage vs Common-Mode Voltage

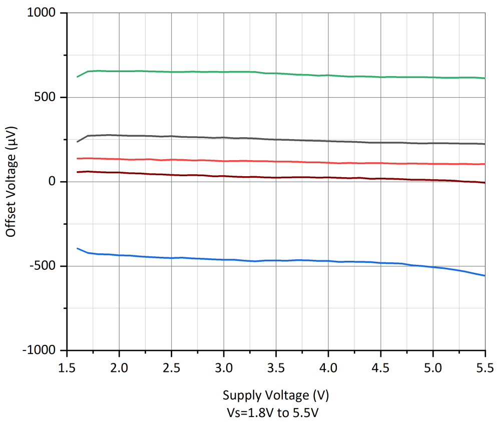


Figure 5: Offset Voltage vs Power Supply

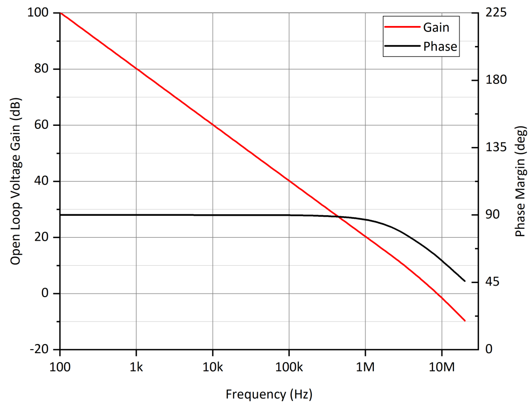


Figure 6: Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

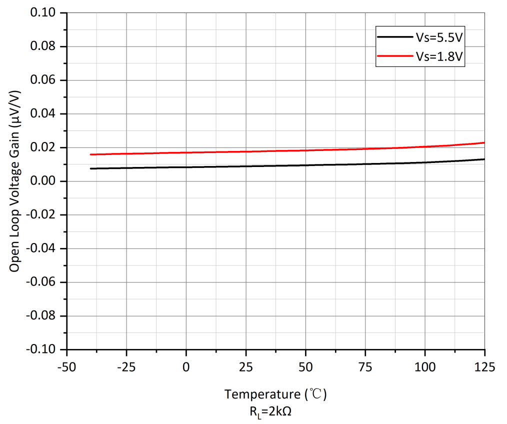


Figure 7: Open-Loop Gain vs Temperature

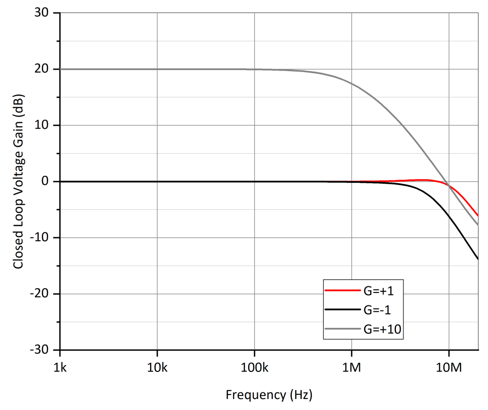


Figure 8: Closed-Loop Gain vs Frequency

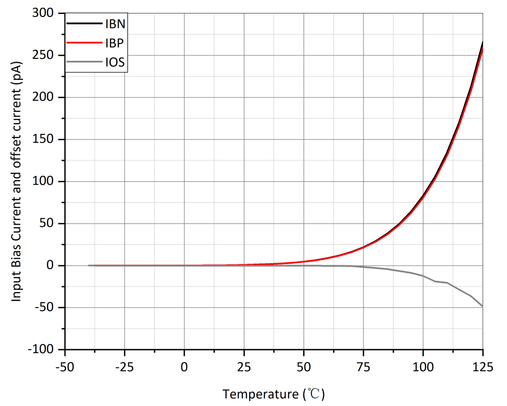


Figure 9: Input Bias Current vs Temperature

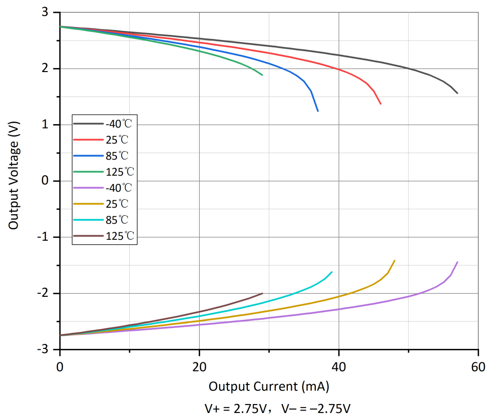


Figure 10: Output Voltage Swing vs Output Current

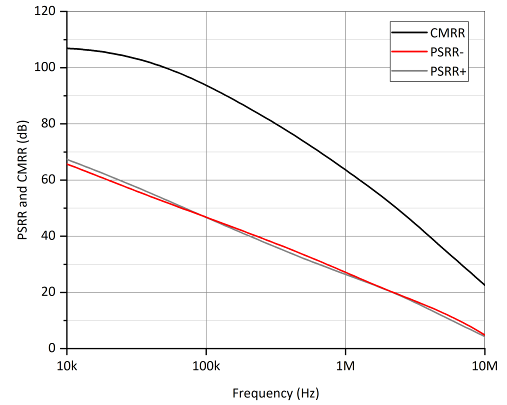


Figure 11: Offset CMRR and PSRR vs Frequency

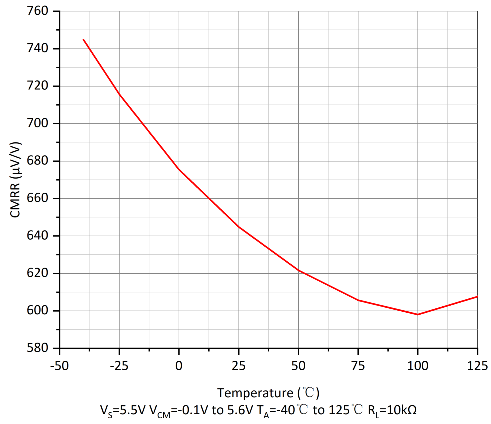


Figure 12: CMRR vs Temperature

Typical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

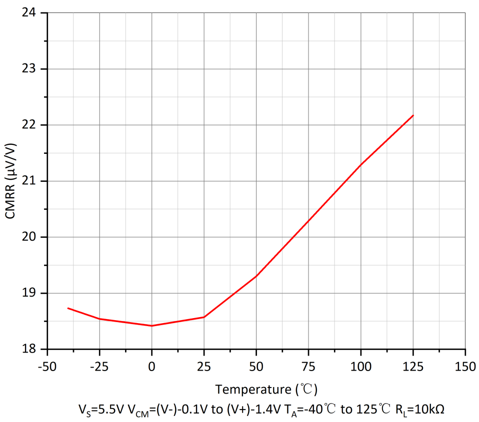


Figure 13: CMRR vs Temperature

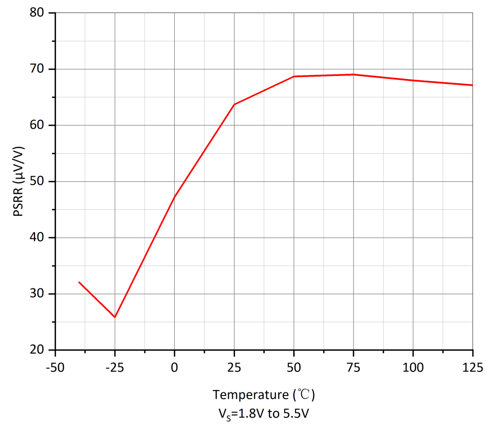


Figure 14: PSRR vs Temperature

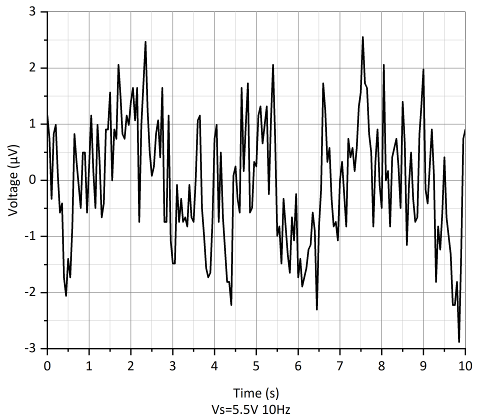


Figure 15: 0.1-Hz to 10-Hz Input Voltage Noise

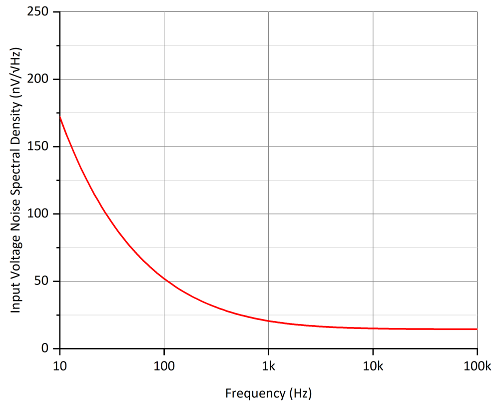


Figure 16: Input Voltage Noise Spectral Density vs Frequency

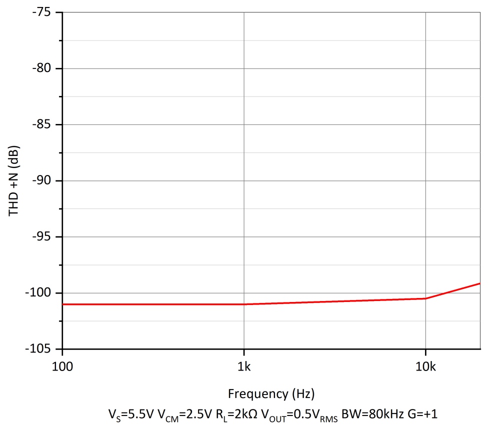


Figure 17: THD + N vs Frequency

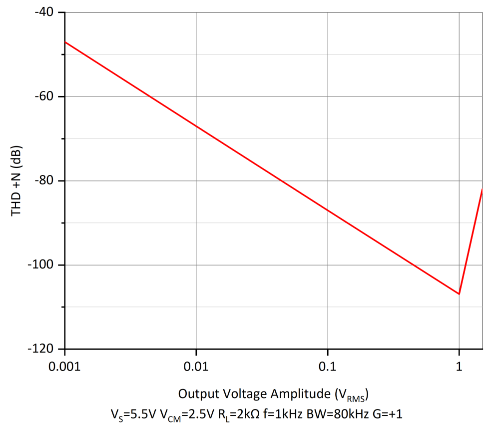


Figure 18: THD + N vs Amplitude

Typical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

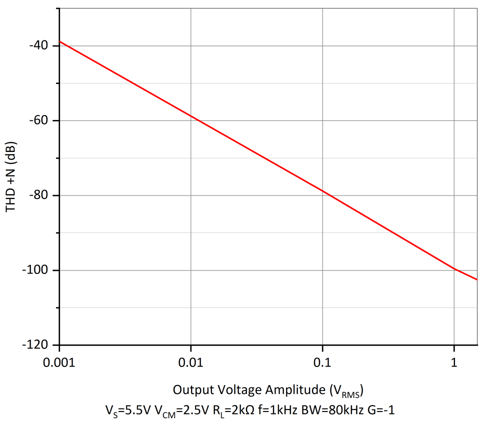


Figure 19: THD + N vs Amplitude

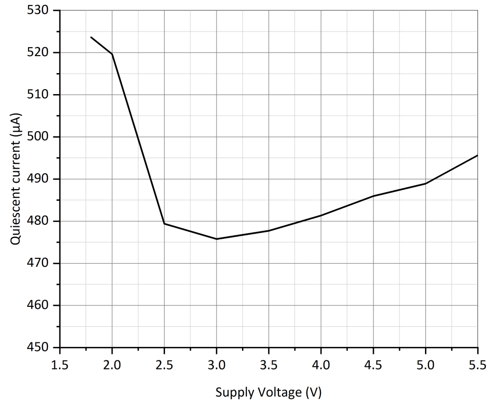


Figure 20: Quiescent Current vs Supply Voltage

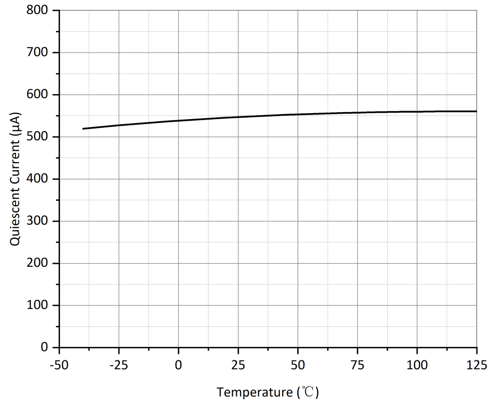


Figure 21: Quiescent Current vs Temperature

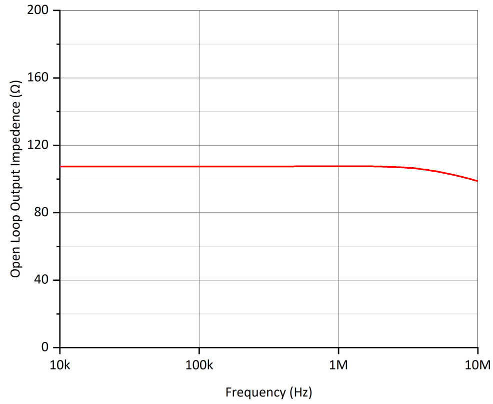


Figure 22: Open-Loop Output Impedance vs Frequency

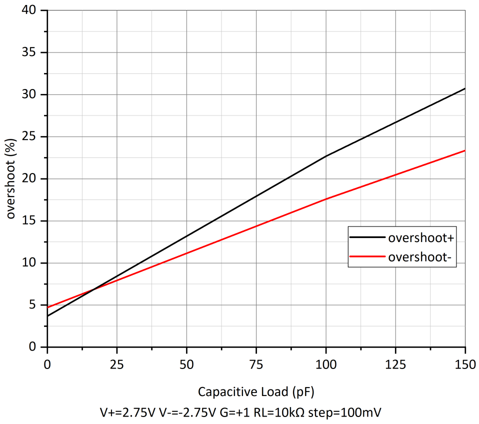


Figure 23: Small-Signal Overshoot vs Load Capacitance

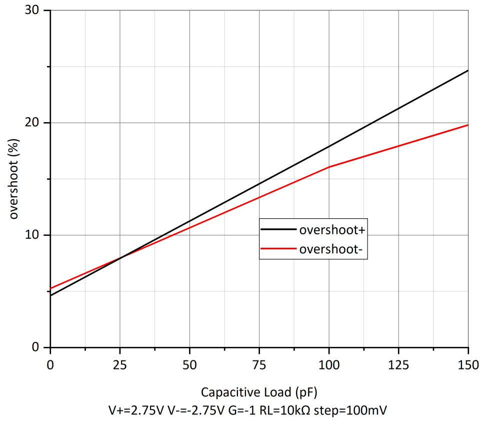


Figure 24: Small-Signal Overshoot vs Load Capacitance

Typical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

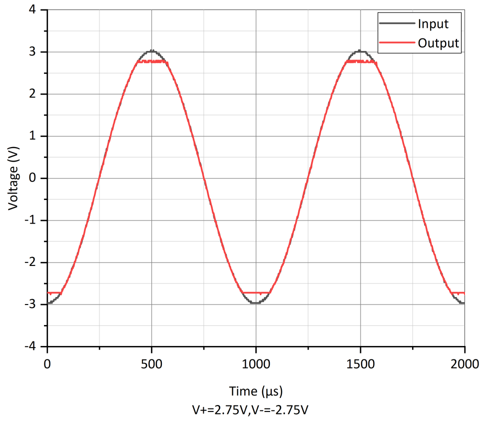


Figure 25: No Phase Reversal

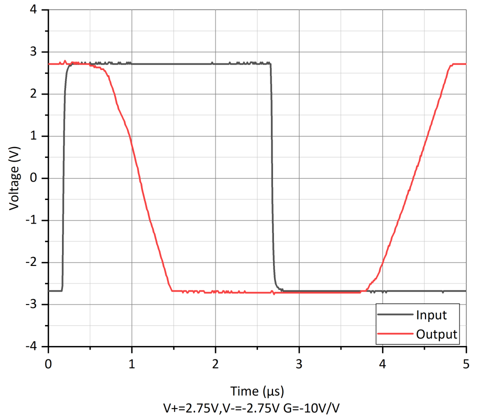


Figure 26: Overload Recovery

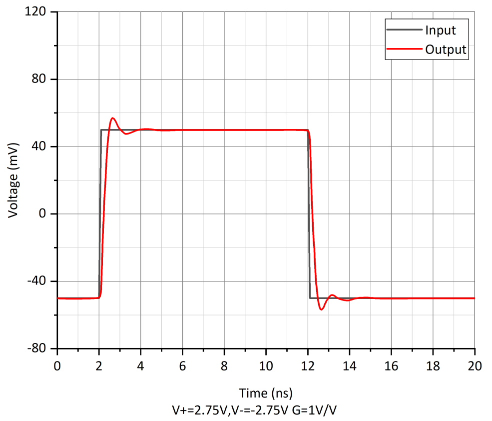


Figure 27: Small-Signal Step Response

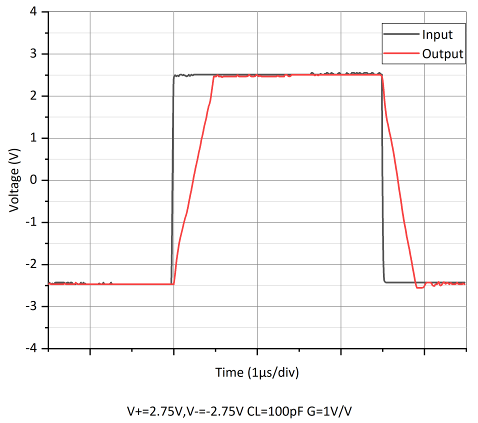


Figure 28: Large-Signal Step Response

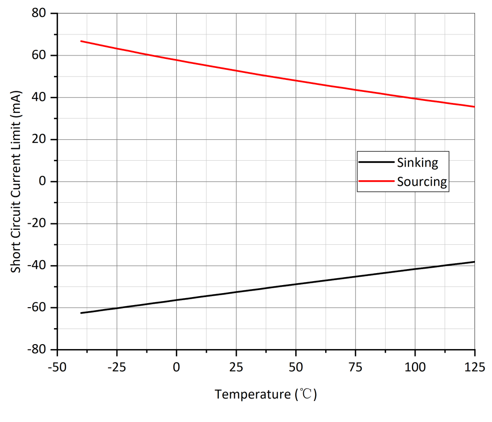


Figure 29: Short-Circuit Current vs Temperature

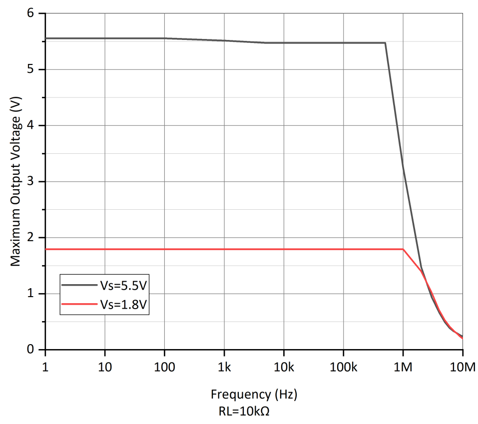


Figure 30: Maximum Output Voltage vs Frequency and Supply Voltage

Typical Characteristics (continued)

For V_S(Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

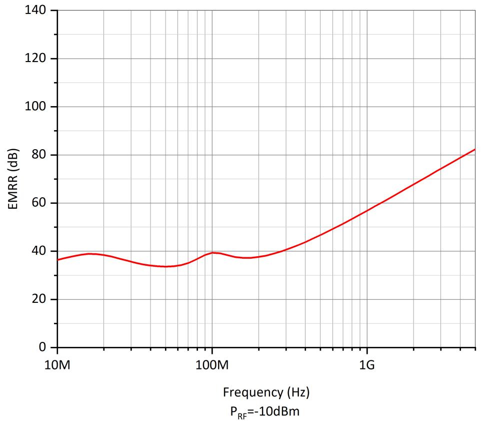


Figure 31: Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

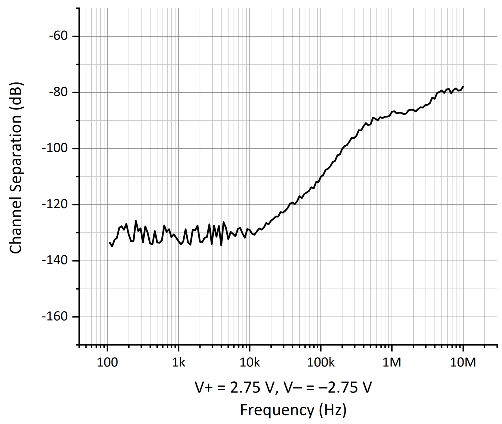


Figure 32: Channel Separation vs Frequency

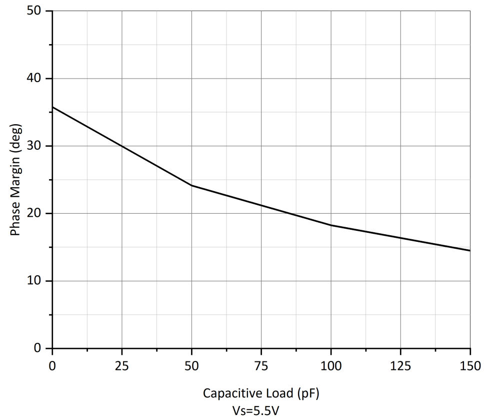


Figure 33: Phase Margin vs Capacitive Load

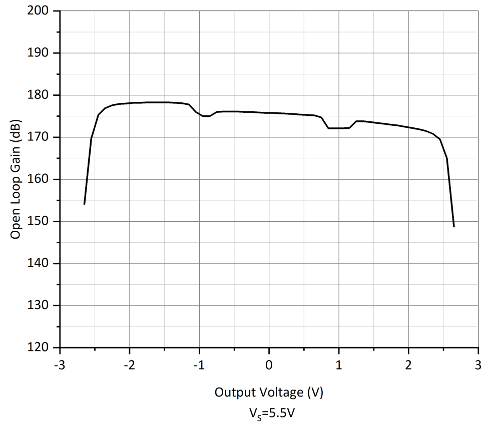


Figure 34: Open Loop Voltage Gain vs Output Voltage

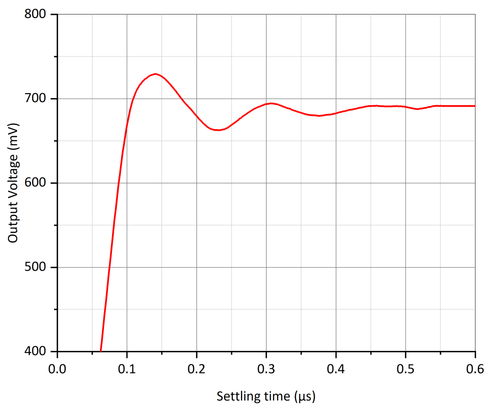


Figure 35: Large Signal Settling Time (Positive)

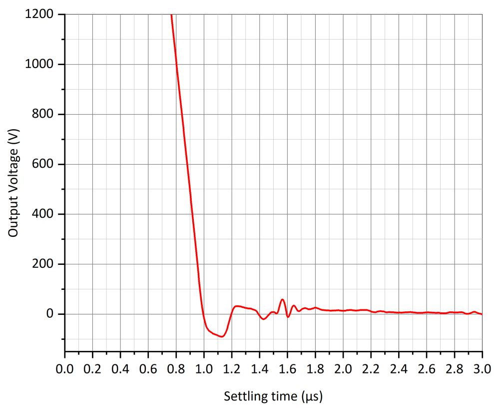


Figure 36: Large Signal Settling Time (Negative)

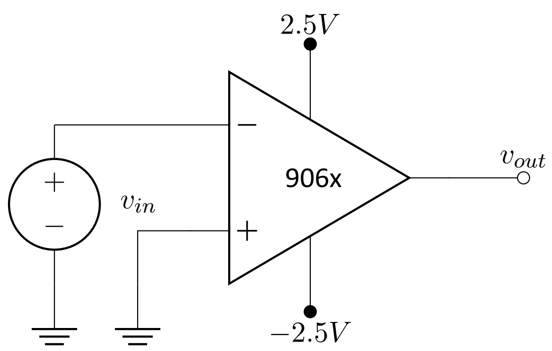
Typical Application

Comparators

Comparators are used to differentiate between two different signal levels. For example, a comparator can be used to differentiate between an overvoltage situation and normal operation. The XMO906x can be used as comparators by applying the two voltages being compared to each input without any feedback from output to inverting input.
The XMO906x features a rail-to-rail input and output stage with an input common-mode range that exceeds the supply rails by 100 mV. The XMO906x is designed to prevent phase reversal over the entire input common-mode range. The propagation delay for the XMO906x used as a comparator is equal to the overload recovery time plus the slew rate. Overdrive voltages less than 100 mV result in longer propagation delays because the overload recovery time increases and the slew rate decreases.

Design Requirements
The design requirements for this design are:
• Supply voltage: ±2.5 V
• Input (VIN): -2.5 V to 2.5 V
• Threshold voltage (VTH): 0 V

Detailed Design Procedure
The inverting comparator circuit applies the input voltage (VIN) to the inverting terminal of the op amp and ground to to the non-inverting terminal of the op amp as threshold voltage. The circuit is shown in following figure. When VIN is less then VTH, the output voltage transitions to the positive supply and equals the high-level output voltage. When VIN is greater than VTH, the output voltage transitions to the negative supply and equals the low-level output voltage.



Application Curves

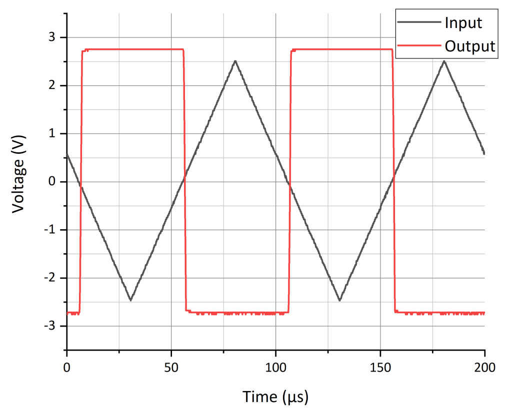


Figure 37: Comparator Response to Input Voltage (Propagation Delay Included)

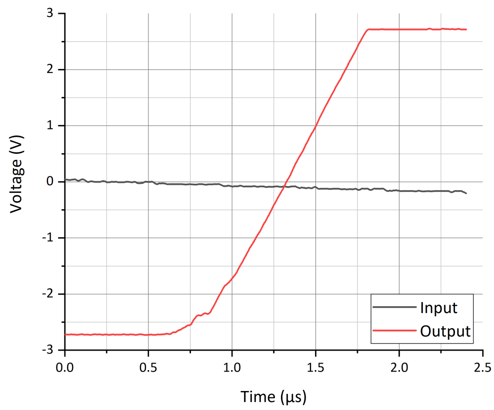


Figure 38: Rising Edge

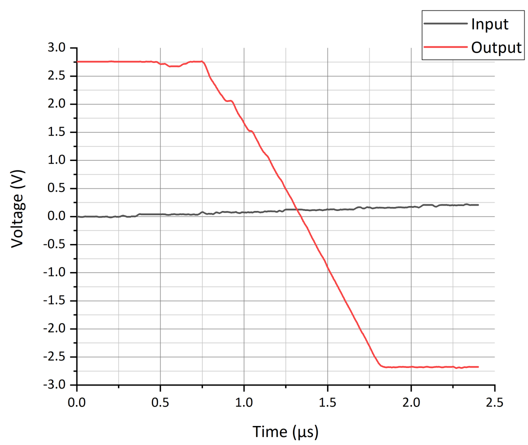


Figure 39: Falling Edge

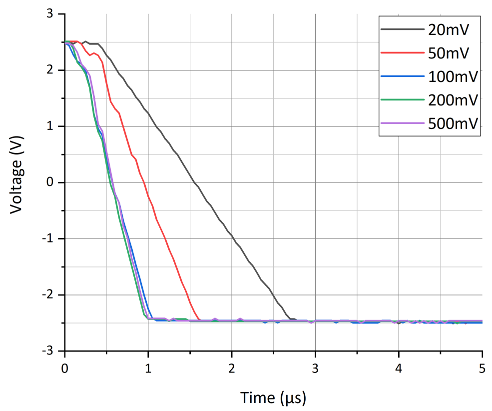


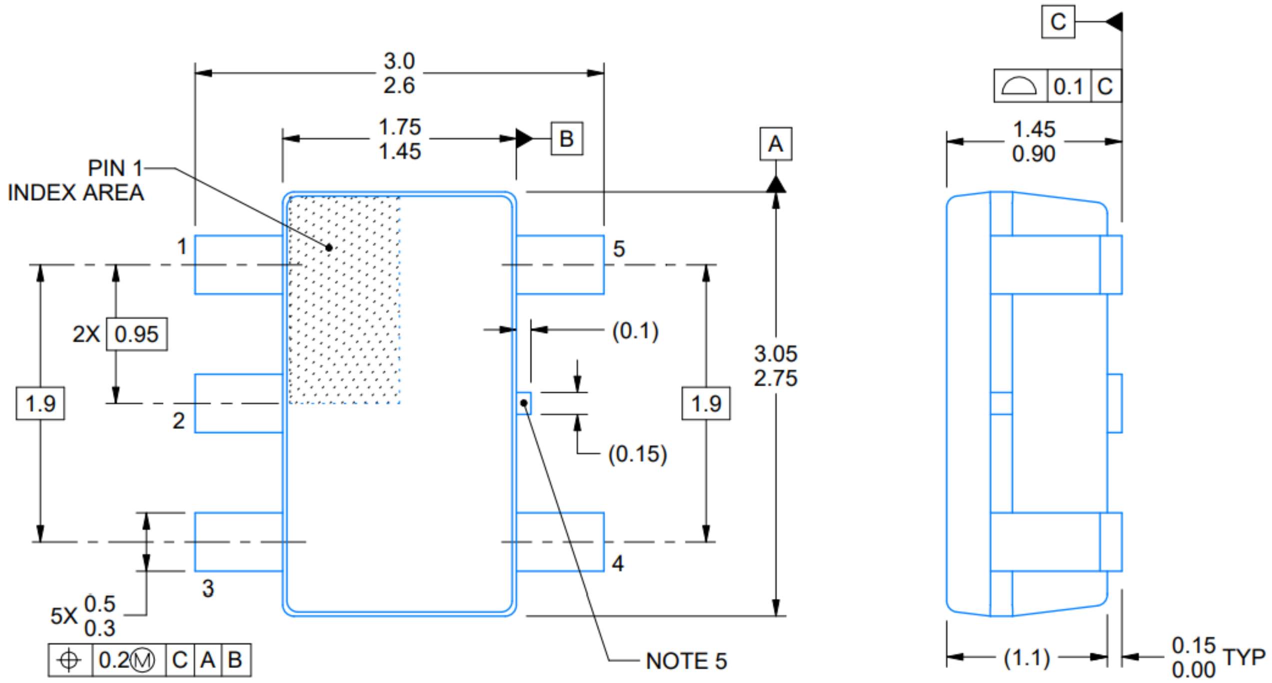
Figure 40: Falling Edge Propagation Delay vsInput Overdrive Voltage

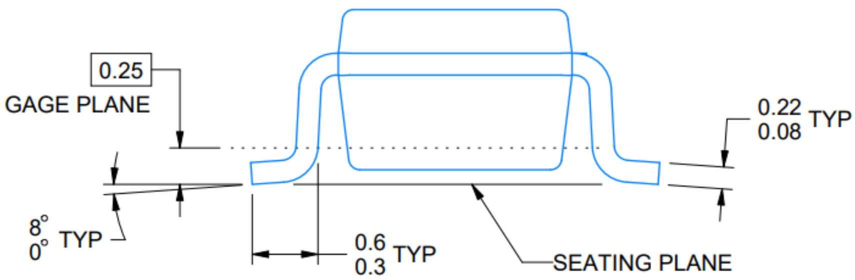
Packaging Infromation

Orderable Device	Status	Package Type	Pins	Package Qty	Eco Plan	Op Temp(°C)	Marking
JML9061IDBVR	ACTIVE	SOT-23	5	4000	RoHS Green	-40 to 125	1S
JML9062IDGKR	ACTIVE	MSOP	8	4000	RoHS Green	-40 to 125	2M
JML9062IDR	ACTIVE	SOP	8	4000	RoHS Green	-40 to 125	2S
JML9064IDR	ACTIVE	SOP	14	2500	RoHS Green	-40 to 125	4S
JML9064IPWR	ACTIVE	TSSOP	14	2500	RoHS Green	-40 to 125	4T

Package Outline Dimension

SOT23-5





NOTE:

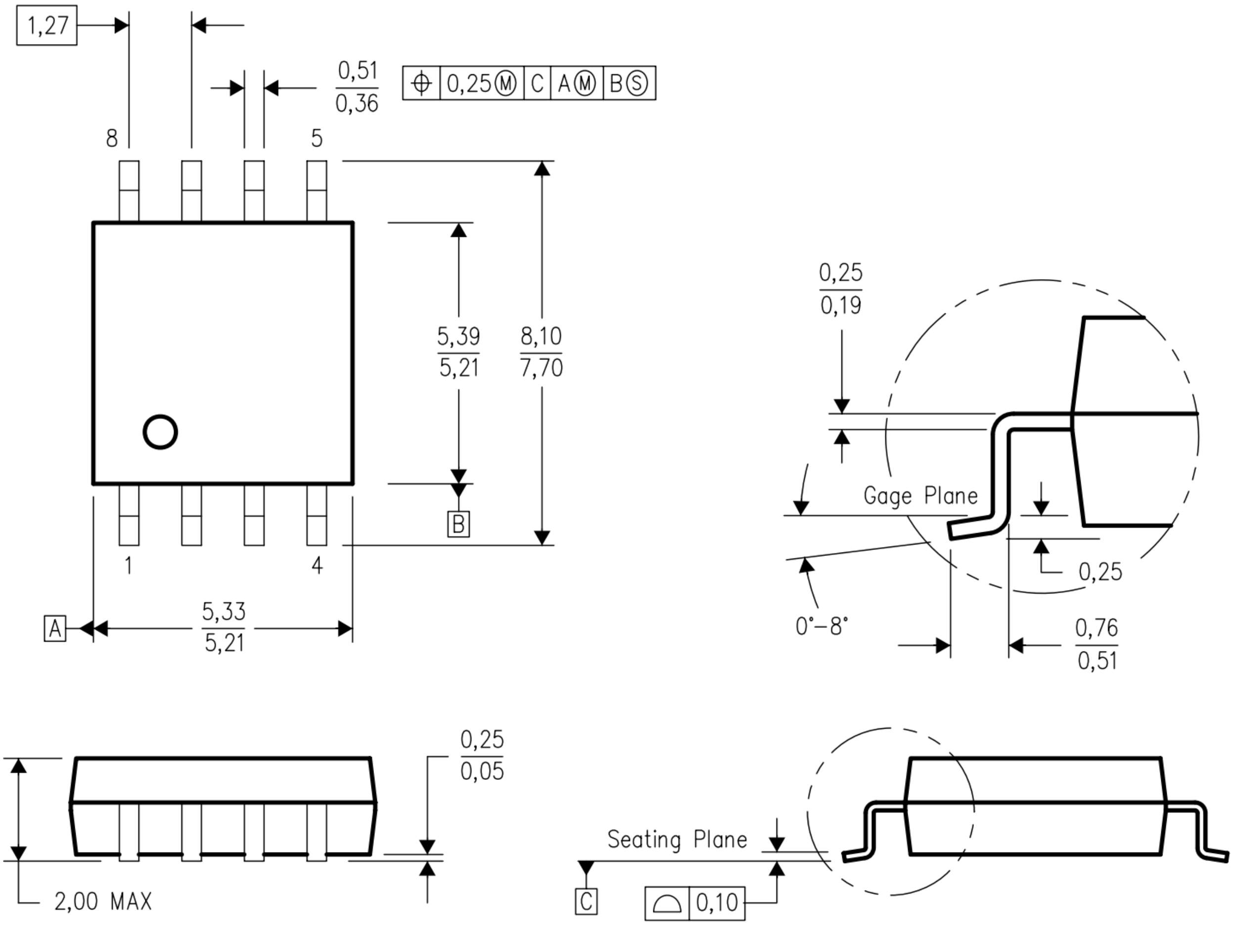
1.All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.

2.This drawing is subject to change without notice.

3.Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

4.Support pin may differ or may not be present.

SOP8



NOTE:

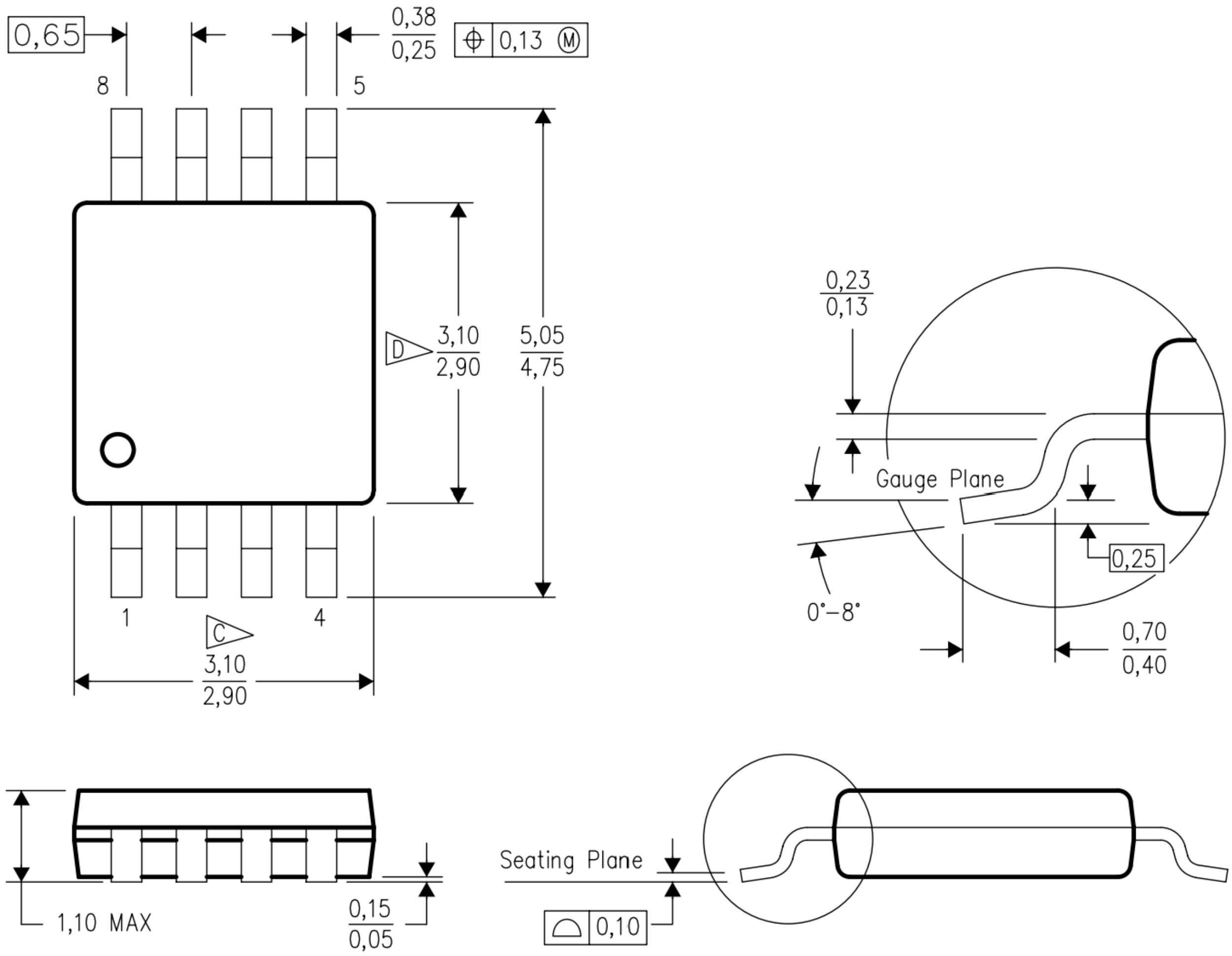
1.All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.

2.This drawing is subject to change without notice.

3.Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

4.Support pin may differ or may not be present.

MSOP8



NOTE:

1.All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.

2.This drawing is subject to change without notice.

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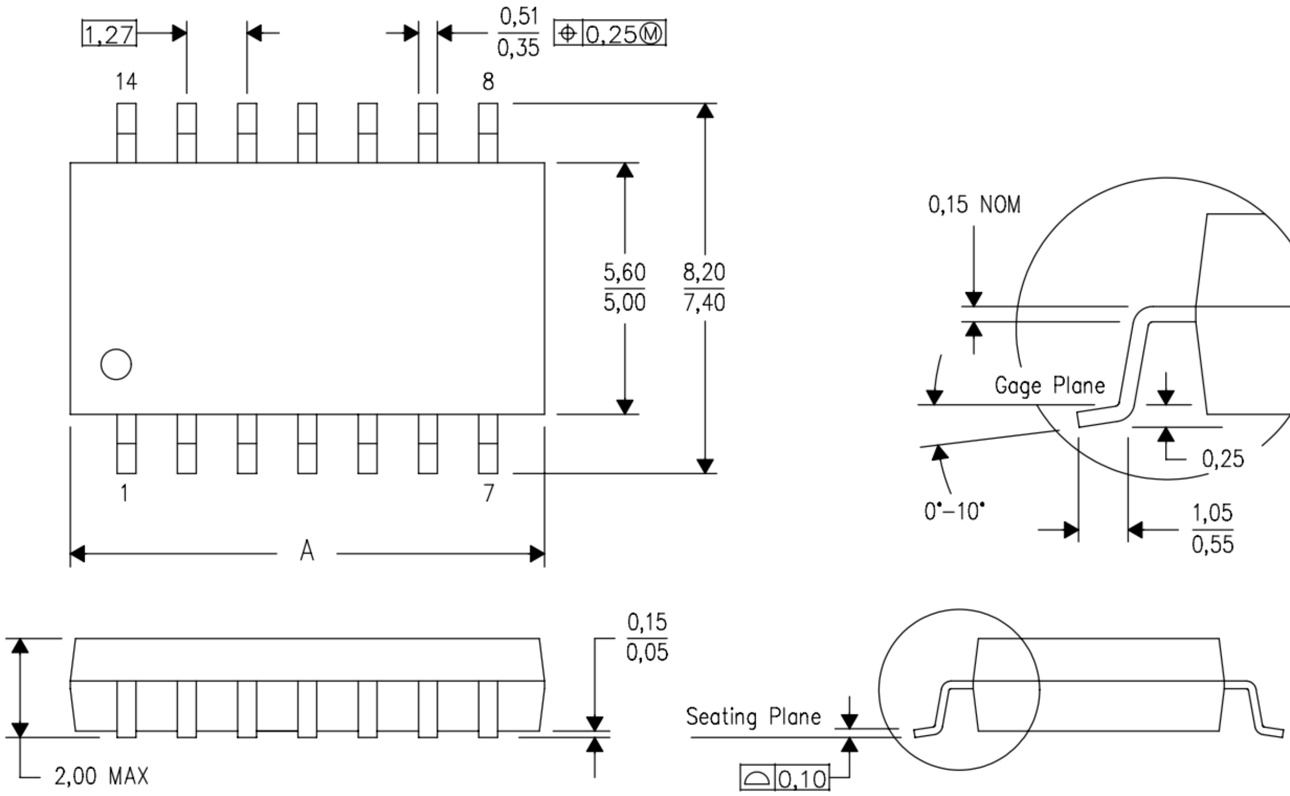
4.Support pin may differ or may not be present.

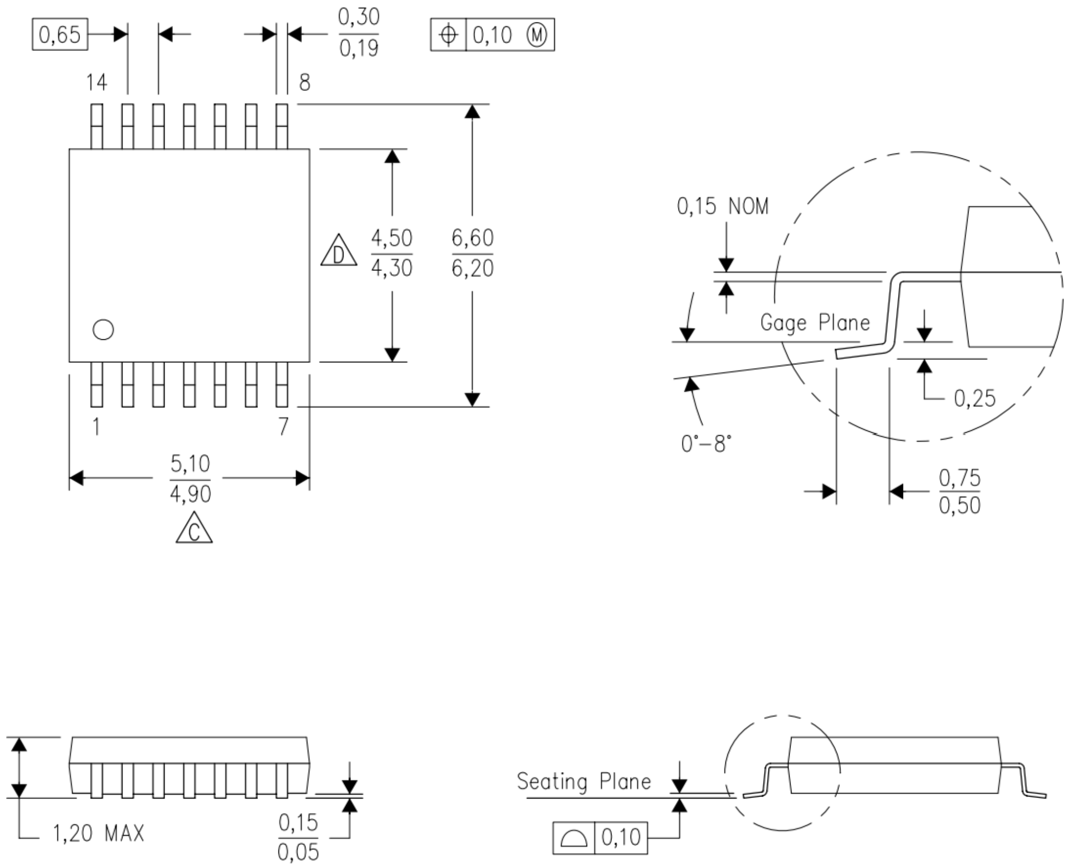
SOP14



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTE:
1.All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
2.This drawing is subject to change without notice.
3.Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
4.Support pin may differ or may not be present.

TSSOP14



NOTE:

1.All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.

2.This drawing is subject to change without notice.

3.Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

4.Support pin may differ or may not be present.